Amendments to the Specification:

Please replace the paragraph beginning at page 9, line 22, with the following rewritten paragraph:

--For the circuits of Embodiments 1-4, F1 = 454545 Hz and F2 = 227582 Hz (all frequencies are rounded to the nearest unit). These frequencies are generated as follows: The PIC16C710 device (U3) generates two frequencies from a 20MHz fixed input frequency. The generated frequencies are 454545 Hz (20 MHZ divided by 44) and 618 Hz (further division by 735). The 618 Hz frequency is fed into a 4048 type PLL phase comparator input. The other phase comparator input of the 4048 type PLL is driven by a PIC12C508 (U2) programmed as a divide-by-368 counter. The relevant input of the PIC12C508 (U2) is the output frequency of the PLL. The circuit of the PIC12C508 and 4048 type PLL is therefore, effectively, a frequency multiplier (or frequency synthesizer), where the output frequency of the PLL is

$$20000000x\frac{368}{44x735} \approx 227582\,\text{Hz}.$$

This is effectively *Fb* from the discussion above.-